CLAIMS

1. A nonvolatile variable resistor comprising: a first electrode and a second electrode facing each other and formed on a substrate; and a nonvolatile variable resistance body formed between the first electrode and the second electrode, characterized in that

the first electrode and the second electrode face each other in a direction of a surface of the substrate.

2. A nonvolatile variable resistor according to claim 1, wherein

the nonvolatile variable resistance body is formed on an outer surface of the first electrode, and the second electrode is formed on an outer surface of the nonvolatile variable resistance body.

3. A nonvolatile variable resistor according to claim 2, wherein

the first electrode is columnar or prismatic.

4. A nonvolatile variable resistor according to claim 3, wherein

the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure.

5. A nonvolatile variable resistor according to claim 4, wherein

the manganese oxide is any of Pr.sub.(1-x)Ca.sub.xMnO.sub.3, La.sub.(1-x)Ca.sub.xMnO.sub.3 and La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3.

6. A nonvolatile variable resistor according to claim 5, wherein

the manganese oxide is any of Pr.sub.0.7Ca.sub.0.3MnO.sub.3, La.sub.0.65Ca.sub.0.35MnO.sub.3 and La.sub.0.65Ca.sub.0.175Pb.sub.0.175MnO.sub.3.

7. A nonvolatile variable resistor according to claim 1, wherein

the first electrode is columnar or prismatic.

8. A nonvolatile variable resistor according to claim 7, wherein

the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure.

9. A nonvolatile variable resistor according to claim 8, wherein

the manganese oxide is any of Pr.sub.(1-x)Ca.sub.xMnO.sub.3, La.sub.(1-x)Ca.sub.xMnO.sub.3 and La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3.

10. A nonvolatile variable resistor according to claim 9, wherein

the manganese oxide is any of Pr.sub.0.7Ca.sub.0.3MnO.sub.3, La.sub.0.65Ca.sub.0.35MnO.sub.3 and La.sub.0.65Ca.sub.0.175Pb.sub.0.175MnO.sub.3.

11. A nonvolatile variable resistor according to claim 1, wherein

the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure.

12. A nonvolatile variable resistor according to claim 11, wherein

the manganese oxide is any of Pr.sub.(1-x)Ca.sub.xMnO.sub.3, La.sub.(1-x)Ca.sub.xMnO.sub.3 and La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3.

13. A nonvolatile variable resistor according to claim

12, wherein

the manganese oxide is any of $Pr_{0.7}Ca_{0.3}MnO_3$, $La_{0.65}Ca_{0.35}MnO_3$ and $La_{0.65}Ca_{0.175}Pb_{0.175}MnO_3$.

14. A memory device having arrangement of memory cells in a matrix on a substrate, each memory cell being constituted of a nonvolatile variable resistor and a selective device, connected to the nonvolatile variable resistor, for selecting the nonvolatile variable resistor, characterized in that

the nonvolatile variable resistor comprises: a first electrode and a second electrode facing each other in a direction of a surface of the substrate and formed on the substrate; and a nonvolatile variable resistance body formed between the first electrode and the second electrode.

15. A memory device according to claim 14, wherein

the nonvolatile variable resistance body is formed on an outer surface of the first electrode, and the second electrode is formed on an outer surface of the nonvolatile variable resistance body.

16. A memory device according to claim 15, wherein

the first electrode is columnar or prismatic.

17. A memory device according to claim 16, wherein the nonvolatile variable resistance body is made of a manganese oxide of a perovskite structure.

18. A memory device according to claim 17, wherein the manganese oxide is any of
Pr.sub.(1-x)Ca.sub.xMnO.sub.3,
La.sub.(1-x)Ca.sub.xMnO.sub.3 and
La.sub.(1-x-y)Ca.sub.xPb.sub.yMnO.sub.3.

19. A memory device according to claim 14, wherein the selective device selects one from the nonvolatile variable resistors to control a current applied to the one of the nonvolatile variable resistors.

20. A memory device according to claim 19, wherein the selective device is a transistor or a diode formed on the substrate.

21. A memory device according to claim 20, wherein the transistor is a MOS transistor, and a drain of the MOS transistor is connected to the first electrode.

22. A memory device according to claim 20, wherein a cathode of the diode is connected to the first electrode.

23. A memory device according to claim 19, wherein the memory cells each have a word line connected to the selective device and a bit line connected to the nonvolatile variable resistor, and the second electrode is connected to the bit line.

24. A memory device according to claim 14, wherein the memory cells each have a word line connected to the selective device and a bit line connected to the nonvolatile variable resistor, and the second electrode is connected to the bit line.

25. A scaling method of a nonvolatile variable resistor including a first electrode and a second electrode facing each other in a direction of a surface of a substrate and formed thereon, and a nonvolatile variable resistance body formed between the first electrode and the second electrode, the method comprising the steps of:

applying reduction scaling to a planar dimension of the first electrode; and

applying magnification scaling to a height dimension of

the first electrode.

26. A scaling method of a nonvolatile variable resistor according to claim 25, wherein

the reduction scaling is applied at a magnification of 1/k times (k > 1), while the magnification scaling is applied at a magnification of k times.